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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/510,567	10/08/2004	Hirohisa Miyazawa	029267.55488US	9020

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/510,567	MIYAZAWA, HIROHISA	
	Examiner	Art Unit	
	Tuan T. Dinh	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Note: Johnson et al. (U.S. Patent 5,025,306) discloses a daughterboard (88) comprising a multilayer, see figures 8-9, column 4, line 3.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Khosrowpour et al. (U.S. Patent 6,477,593)

As to claim 1, Khosrowpour et al. discloses a circuit board device (100) as shown in figures 1-2 comprising:

a base board (110) having a plurality of low-frequency electronic components (see figure 1); and

a multilayer module board (120), which is a low-end module board mounted at one surface and connected to the base board and having a plurality of high-frequency electronic components (see figure 1) including at least a CPU and a memory, wherein

the multilayer module board is smaller in size than the base board (see figure 1), the plurality of high-frequency electronic components are wired to one another through a wiring pattern at an inner layer.

As to claim 5, Khosrowpour et al. discloses the multilayer module board (120) comprising a plurality of high-frequency electronic components including a CPU and a memory mounted at, at least, a surface (top surface) thereof, wherein: the plurality of high-frequency electronic components are connected with one another through a wiring patterns formed at an inner layer thereof (the wiring patterns do not show, but it is inherently that include the wiring patterns in inner layer of the module board 120 for receive or transmit signal data between chip and the CPU).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al. in view of Aruga et al. (U.S. Patent 6,085,137).

As to claim 3, Khosrowpour et al. discloses all of the limitation, except for the device being used in a navigation system.

Aruga et al. teaches a vehicle control device (1) as shown in figure 1 comprising a navigation system (10) comprising at least a power circuit, a gyro and a GPS circuit are mounted at the base board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a teaching of Aruga et al. employed in the device of Khosrowpour et al. in order to provide information and detecting road for the vehicle.

7. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al. in view of Yasuho et al. (U.S. Patent 5,346,402).

Regarding claim 6, Khosrow et al. discloses all of the limitations of the claimed invention, except for connector terminals provided as separate members each soldered onto one of four peripheral edges thereof.

Yasuho et al. shows an insulating substrate (7) having connector terminals (4) provided as separate members each soldered onto one of four peripheral edges, and the substrate (7) connected to a printed wiring board (22), see figure 22.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate as taught by Yasuho et al. employed in the device of Khosrowpour in order to provide a high density electrical connection between board to board.

Regarding claims 7-10, Khosrowpour et al. discloses all of the limitations of the claimed invention, except for connector terminals provided as separate members each soldered onto one of four peripheral edges thereof; the four connector terminals each include; a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion; aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and inclined

surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal; a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

Yasuho et al. shows an insulating substrate (7) having connector terminals (4) provided as separate members each soldered onto one of four peripheral edges, and the substrate (7) connected to a printed wiring board (22), see figure 22; the four connector terminals (14) each include; a narrow, elongated base portion constituted of resin; a plurality of pins fixed to the base portion; aligning pins projecting at both ends of the base portion to be used when soldering the connector terminal onto a rear surface of the board; and inclined surfaces for position control formed at both ends of the base portion to be used when soldering the connector terminal; a pair of positioning holes at which the aligning pins are loosely fitted are formed at each of four corners of the board; and positions of the connector terminals are controlled when soldering the connector terminals as the inclined surfaces for position control at adjacent connector terminals come into contact with each other while the positioning pins are loosely fitted at the positioning holes.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals formed on four peripheral edges of the substrate

as taught by Yasuho et al. employed in the device of Khosrowpour in order to provide a high density electrical connection between board to board.

Response to Arguments

Applicant's arguments filed 07/30/07 have been fully considered but they are not persuasive.

Applicant argues:

a) Khosrowpour does not disclose a daughterboard (120), which is a multilayer board. Examiner disagrees because as taught in Johnson (306) as above, the daughterboard is inherently as a multilayer board.

b) Khosrowpour does not disclose the multilayer board containing at least a CPU and memory. Examiner disagrees because as shown in figure 1 that the daughterboard comprising at least a CPU (a bigger chip, not label) and a memory (the three chip reside near to the square chip (CPU)).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gutierrez F. Diego can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan Dinh
October 12, 2007.

TUAN T. DINH
PRIMARY EXAMINER
10/12/07